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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,798	09/30/2003	T. Warren Weeks JR.	N0400.70001US01	2233

7590 01/14/2005

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EXAMINER	
BLACKWELL RUDASIL, GWENDOLYN A	
ART UNIT	**PAPER NUMBER**
1775	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,798	WEEKS ET AL.	
	Examiner	Art Unit	
	Gwendolyn A. Blackwell-Rudasill	1775	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35,54-67 and 86* is/are pending in the application.

4a) Of the above claim(s) *54-67* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35 and 86* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-35 in the reply filed on October 20, 2004 is acknowledged. The traversal is on the ground(s) that a search and examination of all claims would not place an undue burden on the Examiner. This argument has been considered, but not found persuasive. MPEP § 808.02 recites that for the purposes of the initial requirement of a restriction, a serious burden on the examiner may be prima facie shown if the examiner shows by appropriate explanation either separate classification, separate status in the art, or a different field of search as defined in MPEP § 808.02. Since the Examiner has shown a different classification for the two groups of claims, a burden for examining both groups has been shown.

The requirement is still deemed proper and is therefore made FINAL.

Double Patenting

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101, which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefore ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claims 1, 3, 15, 18-19, 21, 23-32, and 35 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-2, 14, 17-18, 20-21 and 23-27 of prior U.S. Patent No. 6,649,287. This is a double patenting rejection.

Ultimately, forming an FET is seen as intended use, which does not patentably distinguish the structure of the claimed subject matter over the structure of the prior art of record.

4. Claim 32 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of prior U.S. Patent No. 6,617,060. This is a double patenting rejection.

Ultimately, forming an FET is seen as intended use, which does not patentably distinguish the structure of the claimed subject matter over the structure of the prior art of record.

Claim Objections

5. Claims 4, 12, 16-17, 20, and 34 are objected to because of the following informalities:

The range of the a, b, x, and y parameters need to included in the claims to clearly delineate the metes and bounds of those parameters. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> *The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.*

7. Claims 9 and 33-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 9 recited the limitation "the transition layer comprises $Al_xIn_{1-x}N$" in the first line. There is insufficient antecedent basis for this limitation in the claim. Claim 6 is dependent from

claim 4 which has consisting of language limiting the alloys of gallium nitride to those listed in claim 4.

9. Claims 33-34 recites the limitation "the intermediate layer" in the first line of each claim. There is insufficient antecedent basis for this limitation in the claim. Claim 1 does not disclose an intermediate layer.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-29, and 32-35 under 35 U.S.C. 102(b) as being anticipated by United States Patent no. 5,874,747, Redwing et al.

Regarding claims 1-8, 10-14, 19, and 35

Redwing discloses a GaN alloy layer grown on a substrate that can be SiC or Si with a transition layer grown between the substrate and the GaN layer, meeting the requirements for claims 1, 19, and 35, (column 4, lines 62-65). The composition of the transition layers can be continuous along the thickness or graded stepwise or incrementally, meeting the requirements for claims 2-3 and 14, (column 22, lines 39-47). The transition layer comprises gallium nitride, which is compositionally graded comprising the formulas $Al_xGa_{1-x}N$ where the value of x ranges from 0 to 1. The value of x can be 0 to 1 starting from the substrate or 1 to 0 starting from the substrate, meeting the requirements of claims 4-8 and 11-13, (column 7, lines 15-30). The

composition of gallium nitride can also be $In_xGa_{1-x}N$ with the range of $0.05<x<0.5$ and $Al_yGa_{1-y}N$ where y ranges between 0 to 0.3, meeting the requirements of claim10, (column 14, lines 18-22).

Regarding claims 15-17 and 20

Redwing also discloses that the gallium nitride may be a superlattice such as $M_{1-x-y}M'_yGa_xN$ wherein x and y range from 0 to 1 and M is a metal compatible with Ga and N and M' is a compatible metal providing quaternary compounds such as AlInGaN, meeting the requirement of claims 15-17 and 20, (column 14, lines 46-68; see also claims 25-30).

Regarding claims 9, 18, 21-24, 26-29, and 32-34

Redwing further discloses that the transition layer has a thickness between 200 angstroms to 5 μm, meeting the requirements of claims 18 and 21, (column 7, lines 30-32). The invention of Redwing can be a LED, LD, or semiconductor device, meeting the requirements of claims 22-24, (column 9, lines 55-60). The present invention has a structure, which eliminates cracking, meeting the requirements of claims 26-28, (column 18, lines 53-56). The gallium nitride layer is single crystal, meeting the requirements claim 29, (column 22, lines 21-23). An intermediate layer may be placed between the substrate and the transition layer, meeting the requirements of claim 32, (column 19, lines 23-29). The intermediate layer can be a thin layer of AlN, or can be comprised of a thin compositionally graded buffer layer alloy of gallium nitride such as (Al, In)N, (Al, Ga)N, (Al, Ga, In)N, (In, Ga)N, meeting the requirements of claims 9 and 33-34, (columns 19-20, lines 23-19).

Regarding claim 25

The phrase "wherein the semiconductor material forms a FET" is considered a statement of intended use. The intended use of the claimed invention must result in a structural difference

between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Because the layer structure of Redwing et al is not structurally different from the semiconductor material as claimed by Applicant, the semiconductor material as claimed does not provide patentable distinction over the prior art of record.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 25, 30-31, and 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent no. 5,874,747, Redwing et al as applied to claims 1 and 22 above, in view of

United States Patent no. 6,426,512 B1, Ito et al further in view of United States Patent no. 6,287,947, Ludowise et al.

Redwing et al disclose the limitations of claims 1 and 22 above. Redwing et al also disclose that the invention can be a LED, LD, or semiconductor device, (column 9, lines 55-60). The present invention has a structure that eliminates cracking, (column 18, lines 53-56). Redwing et al do not specifically disclose that the semiconductor device is an FET or the size of the substrate as exemplified by Applicant or that the silicon substrate is textured.

Ito et al disclose a semiconductor device that utilizes a group III nitride compound, such as GaN and it's alloys, wherein the substrate can be SiC or Si, (column 4, lines 50-67). Ito et al. also disclose that a "FET structure can be also formed from group III nitride compound semiconductors," (column 8, lines 56-65). Between the substrate and the GaN layer is an undercoat layer and a buffer layer, wherein the buffer layer is $Al_aGa_{1-a}N$ ($0 \leq a \leq 1$), (column 16, lines 65-67). The thickness of the substrate can be 300 μm, (column 13, examples).

Ludowise et al disclose structures related to GaN based LEDs and LDs comprised of a substrate and a number of layers, (column 5, lines 47-48). The substrate can be comprised of silicon containing materials wherein the surface of the substrate is textured, (column 5, lines 51-56).

Redwing et al, Ito et al, and Ludowise et al are commensurate in scope in that the aforementioned inventions are related to better ways to improve the lattice mismatch between the GaN layer(s) and the substrate. It is known in the art that Si, SiC, and sapphire can be used as substrates in the manufacturing of FETs, LDs, and LEDs. It is also known that there the lattice mismatch between GaN and a Si or SiC substrate can be decreased by the use of a buffer layer,

(Redwing, col. 4, lines 62-65). It is also known that Si is less expensive than SiC when used a substrate for a semiconductor device. Therefore it would have been obvious to one skilled in the art at the time of invention to modify the semiconductor device of Redwing with the Si substrate of Ito to create a FET that is less expensive to manufacture. It would also be within the skill of one in the are at the time of invention to modify the substrate of the Redwing/Ito invention in order to randomize the incident light and increase the probability of incident light escaping the LED through the sides or upper surface of the semiconductor region, (column 5, lines 47-62).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to adjust the diameter of the substrate through routine experimentation in order to achieve a semiconductor device that has improved structural and optical properties. It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gwendolyn A. Blackwell-Rudasill whose telephone number is (571) 272-1533. The examiner can normally be reached on Monday - Thursday; 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Deborah Jones can be reached on (571) 272-1535. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gwendolyn A. Blackwell-Rudasill
Examiner
Art Unit 1775

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